FIG. 1

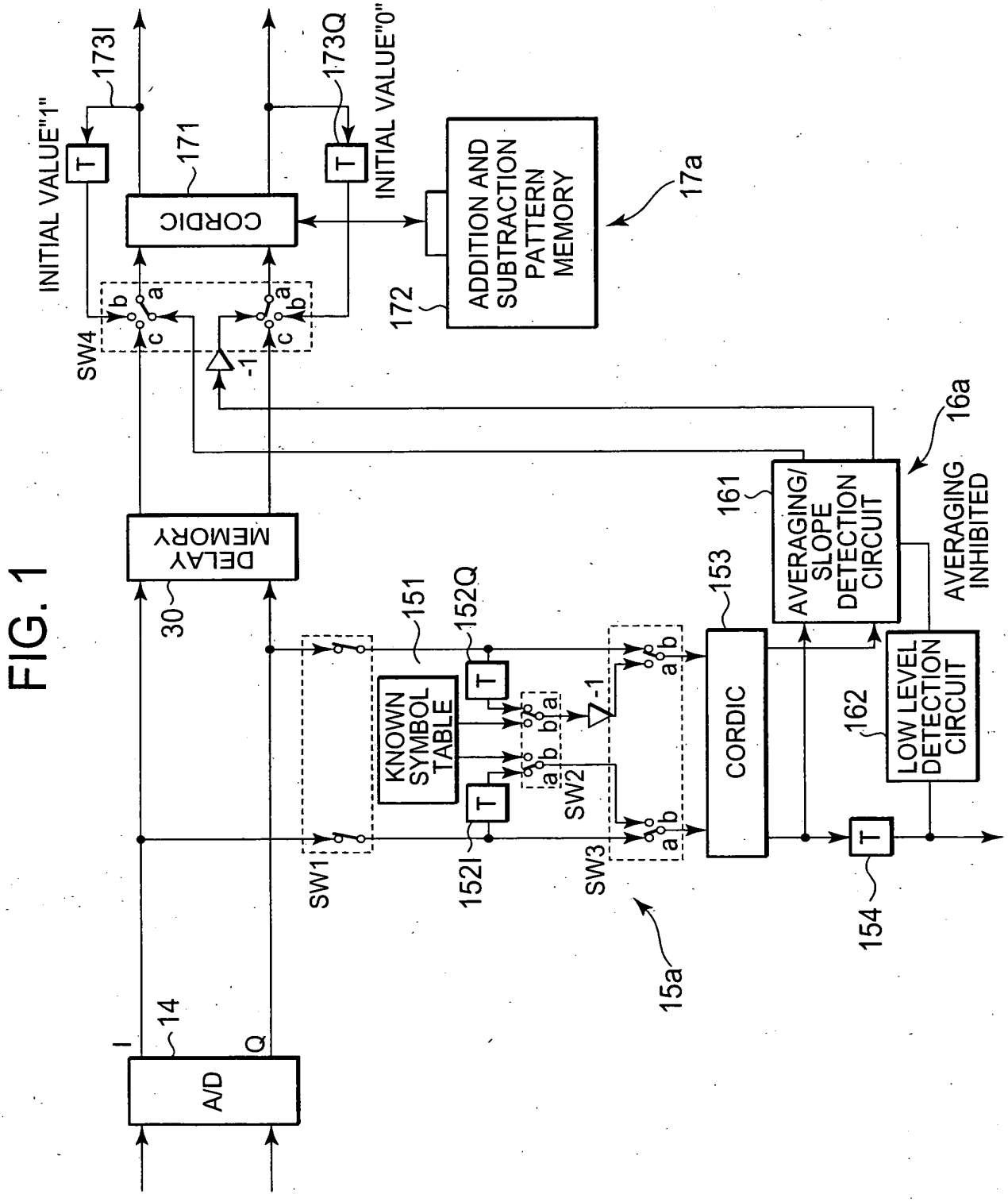
A/D
14
I
Q
DELAY MEMORY
30
SW1
KNOWN SYMBOL TABLE
151
152I
152Q
T
SW2
-1
SW3
15a
CORDIC
153
AVERAGING/ SLOPE DETECTION CIRCUIT
161
16a
AVERAGING INHIBITED
LOW LEVEL DETECTION CIRCUIT
162
154
SW4
CORDIC
171
173I
173Q
INITIAL VALUE"1"
INITIAL VALUE"0"
ADDITION AND SUBTRACTION PATTERN MEMORY
172
17a

FIG. 2

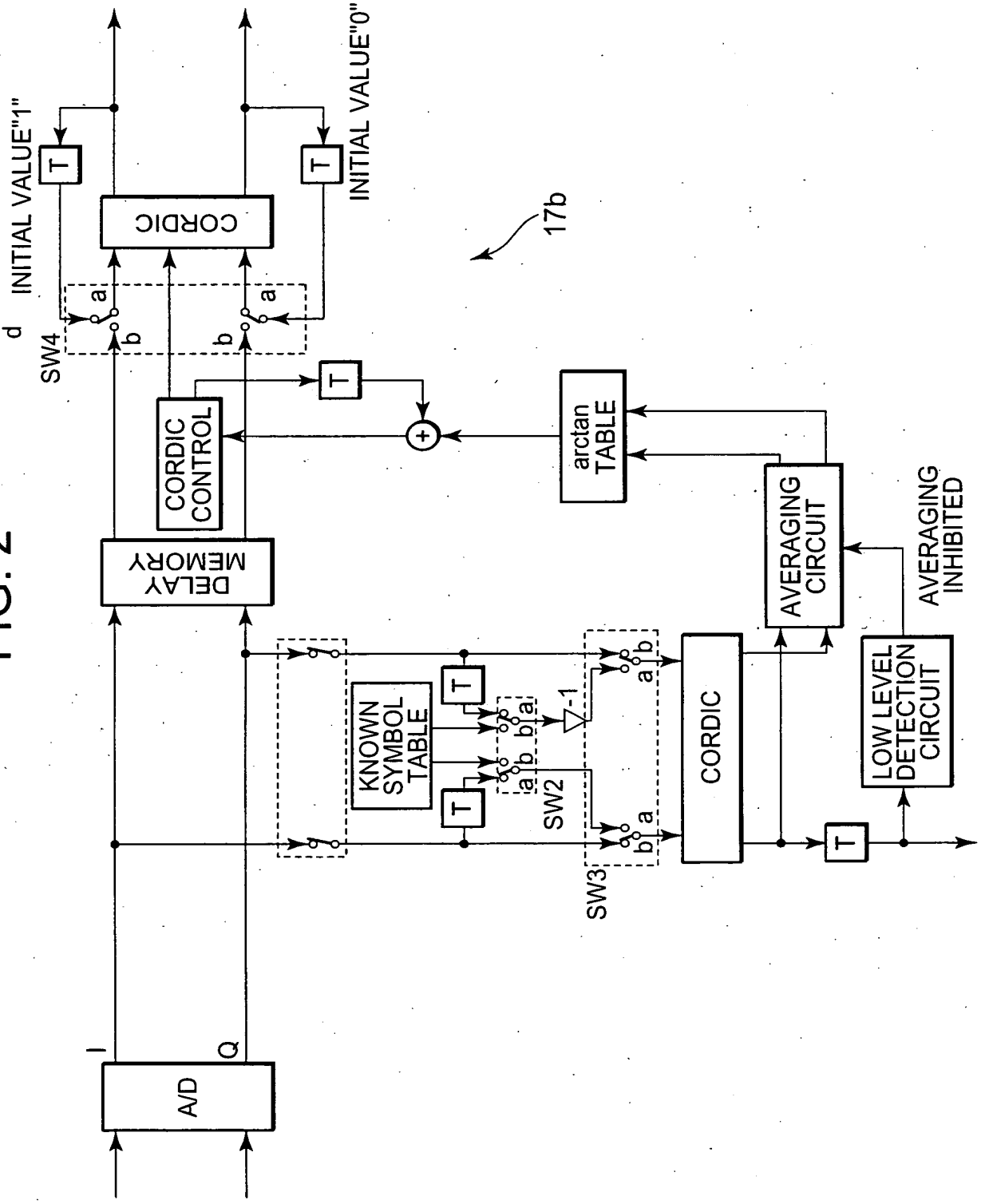
17b
INITIAL VALUE"1"
INITIAL VALUE"0"
d
SW4
a
b
T
CORDIC
CORDIC CONTROL
arctan TABLE
DELAY MEMORY
AVERAGING CIRCUIT
AVERAGING INHIBITED
KNOWN SYMBOL TABLE
SW2
SW3
-1
CORDIC
LOW LEVEL DETECTION CIRCUIT
A/D
I
Q

FIG. 3

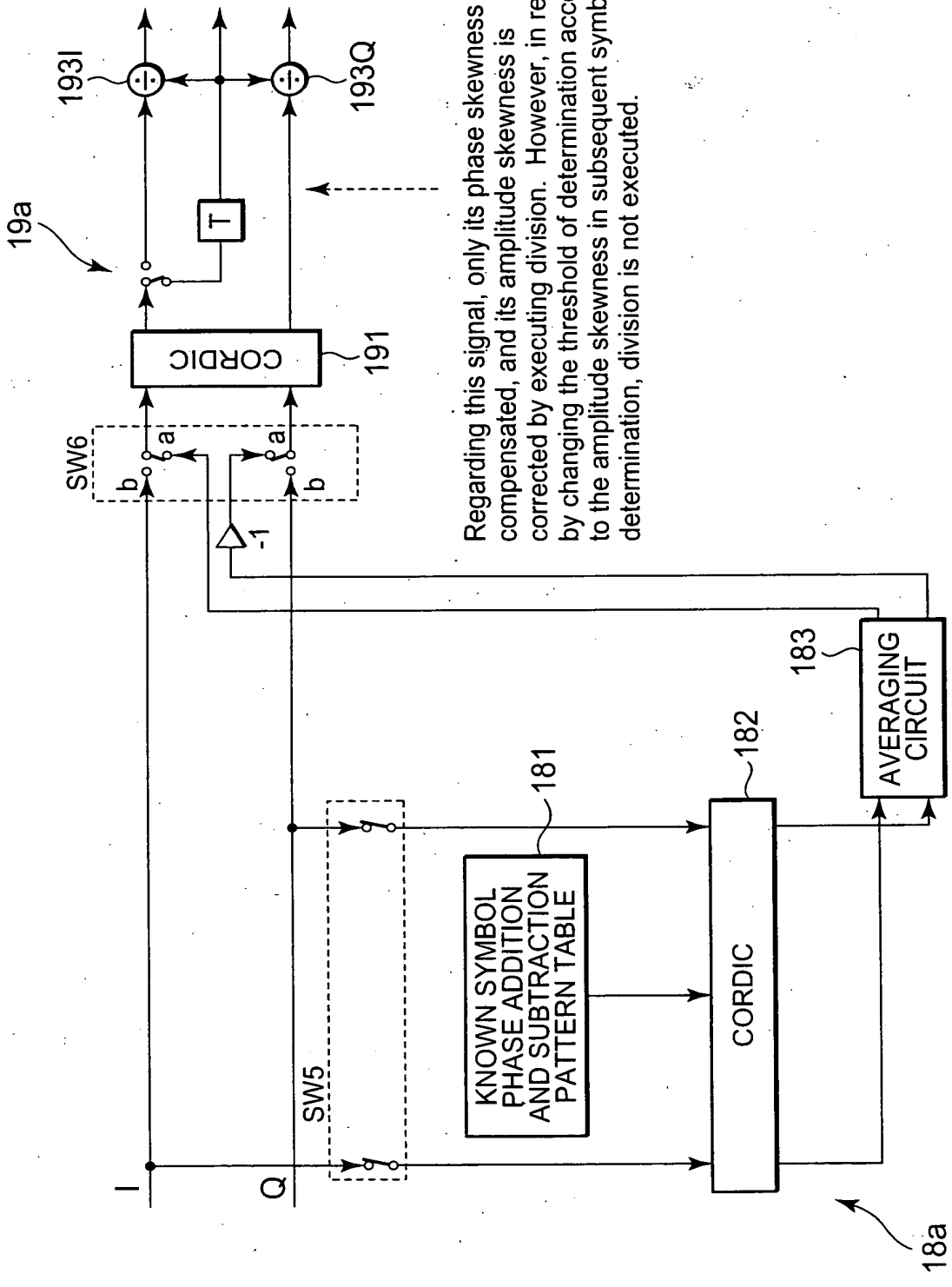
193I
193Q
19a
T
CORDIC
191
SW6
a
b
-1
Regarding this signal, only its phase skewness is compensated, and its amplitude skewness is corrected by executing division. However, in reality, by changing the threshold of determination according to the amplitude skewness in subsequent symbol determination, division is not executed.
183
AVERAGING CIRCUIT
182
181
KNOWN SYMBOL PHASE ADDITION AND SUBTRACTION PATTERN TABLE
CORDIC
SW5
I
Q
18a
Though a CORDIC output is a value obtained by multiplying a true value of quotient by root (Pr^2+Pi^2)(constant number multiplication), there is no problem.

FIG. 4

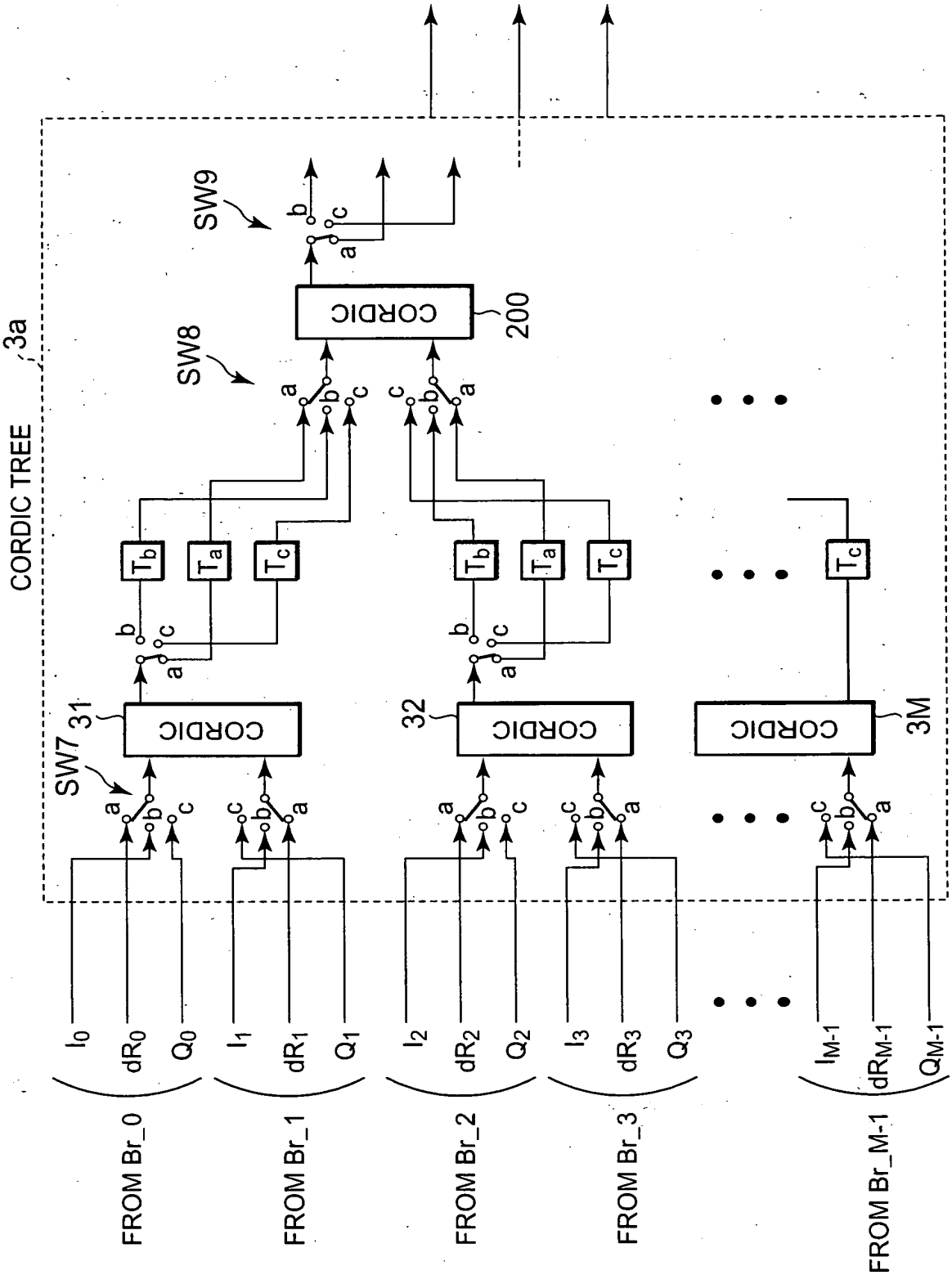
CORDIC TREE
3a
SW9
SW8
SW7
CORDIC
200
31
32
3M
Ta
Tb
Tc
a
b
c
I0
dR0
Q0
I1
dR1
Q1
I2
dR2
Q2
I3
dR3
Q3
IM-1
dRM-1
QM-1
FROM Br_0
FROM Br_1
FROM Br_2
FROM Br_3
FROM Br_M-1

FIG.5

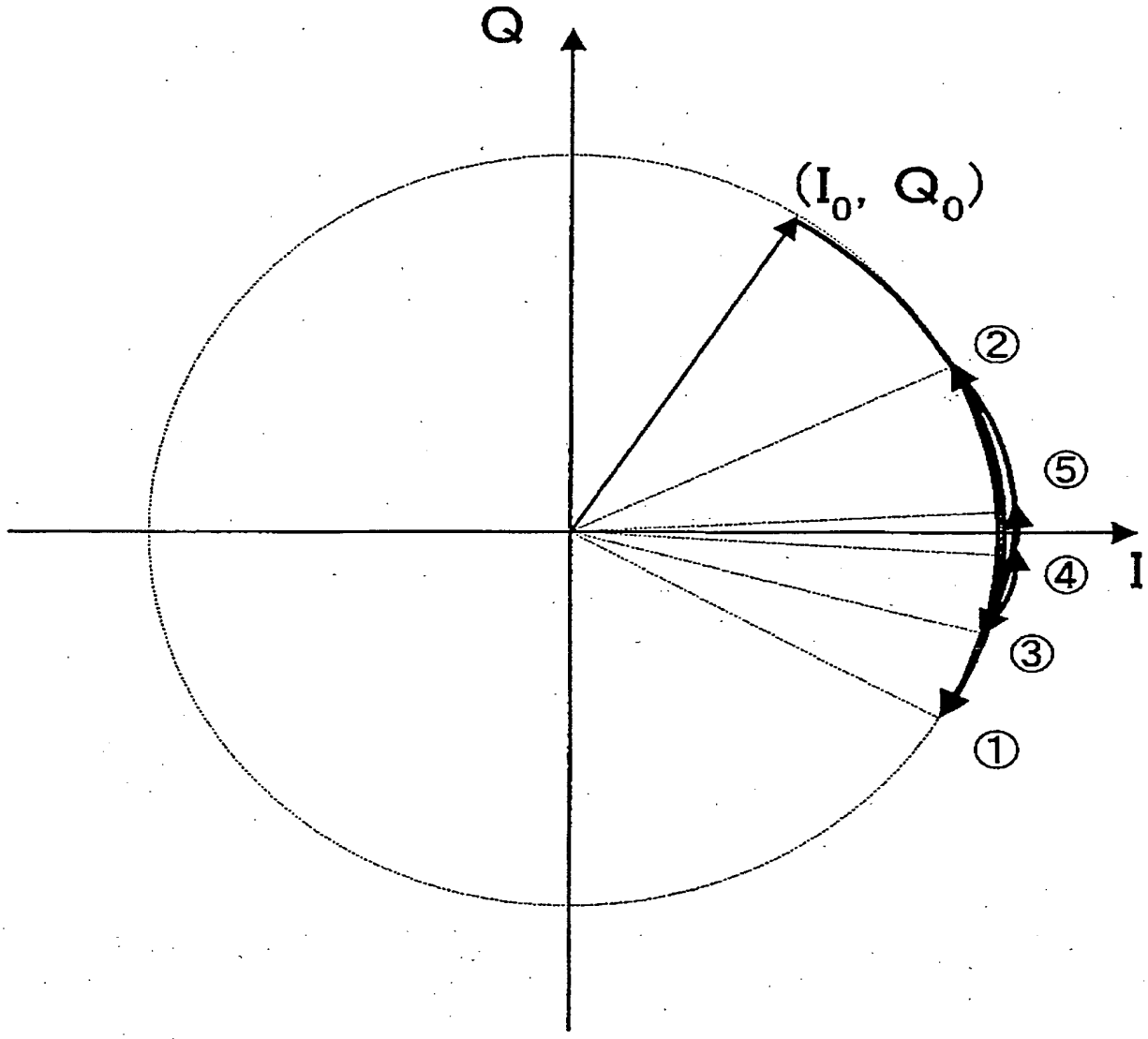

FIG. 6A

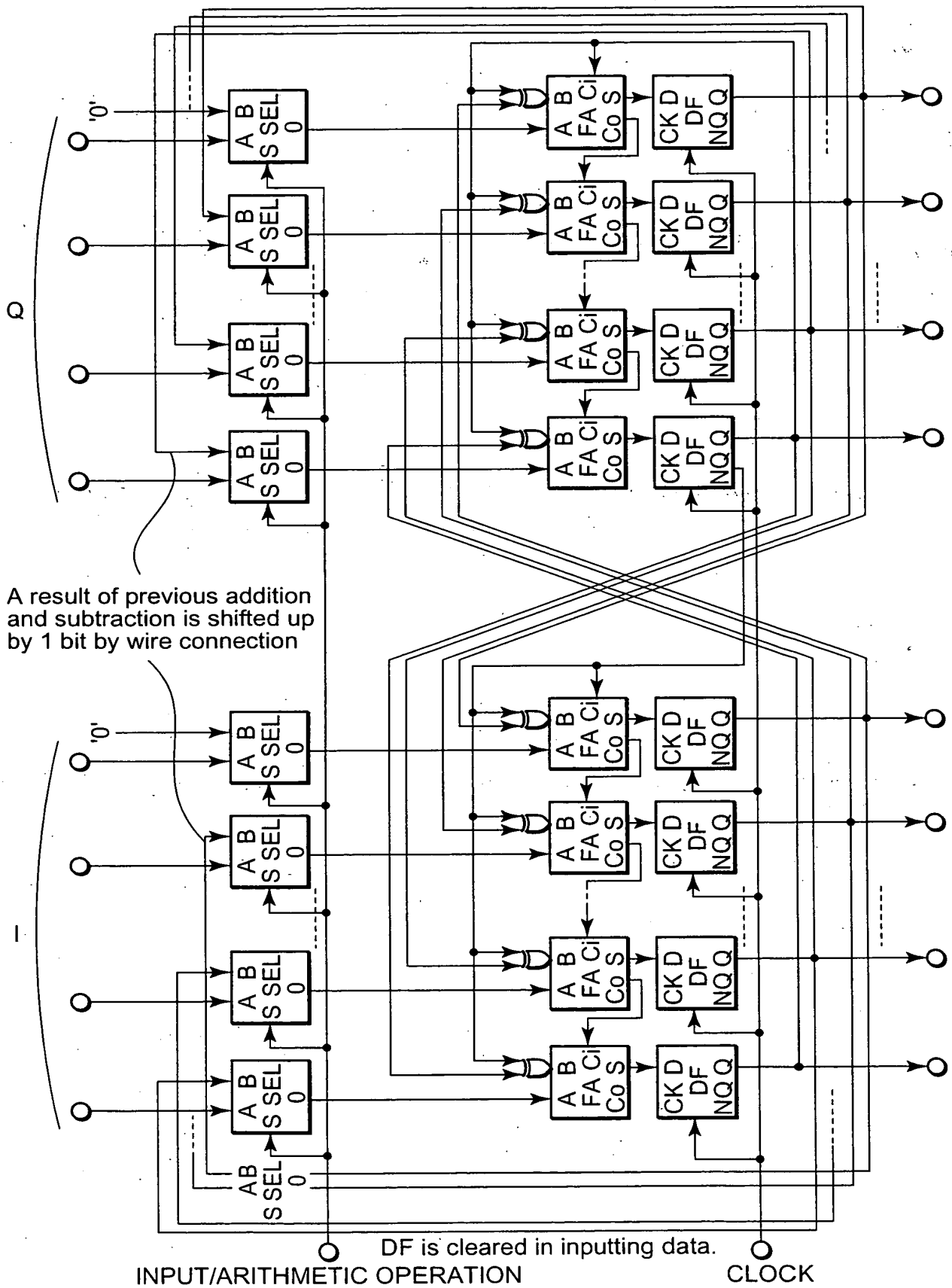
'0'
Q
A result of previous addition and subtraction is shifted up by 1 bit by wire connection
'0'
I
A B S SEL 0
A B FA Ci Co S
CK D DF NQ Q
AB SEL 0
DF is cleared in inputting data.
INPUT/ARITHMETIC OPERATION
CLOCK

FIG.6B

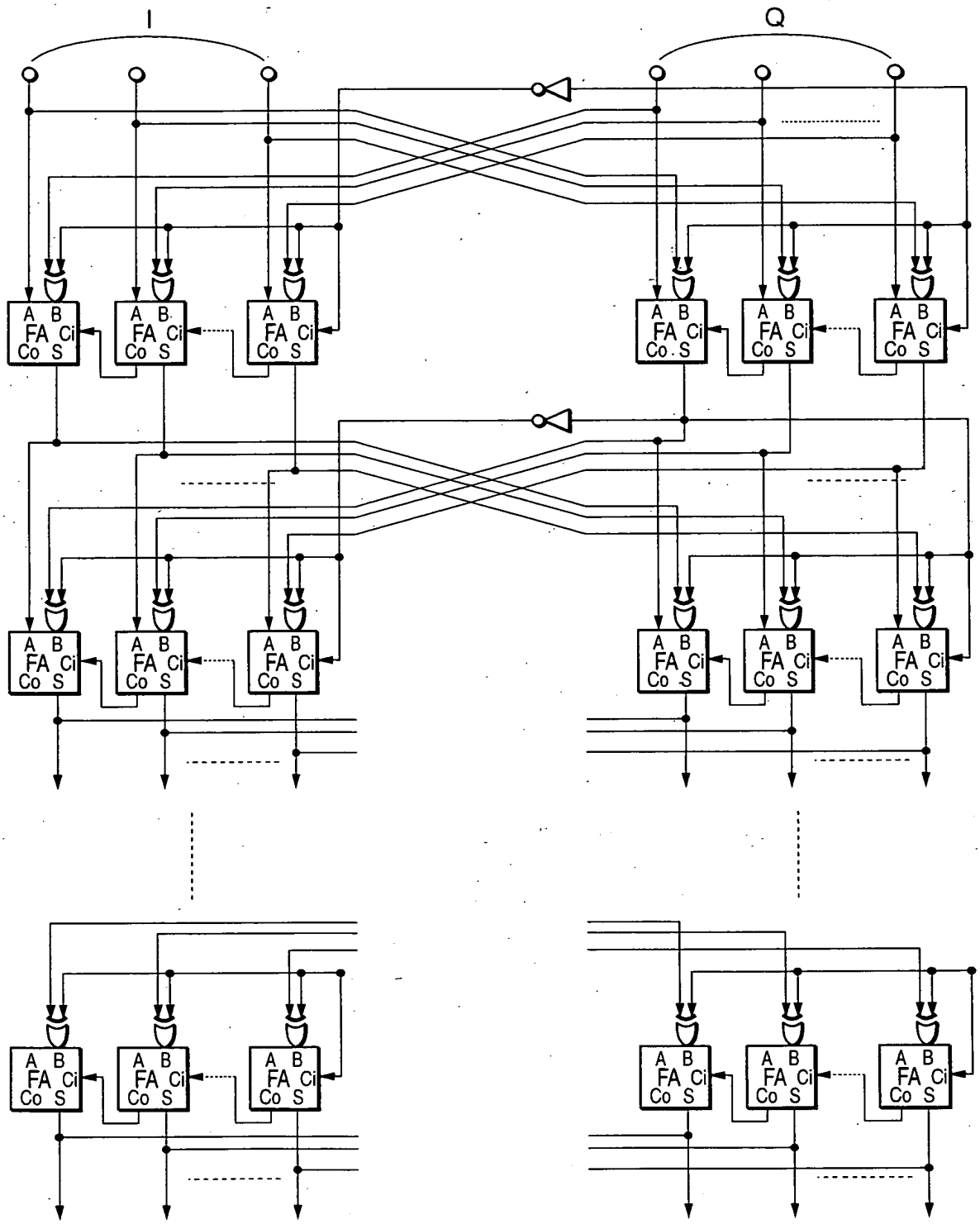

FIG. 7 PRIOR ART

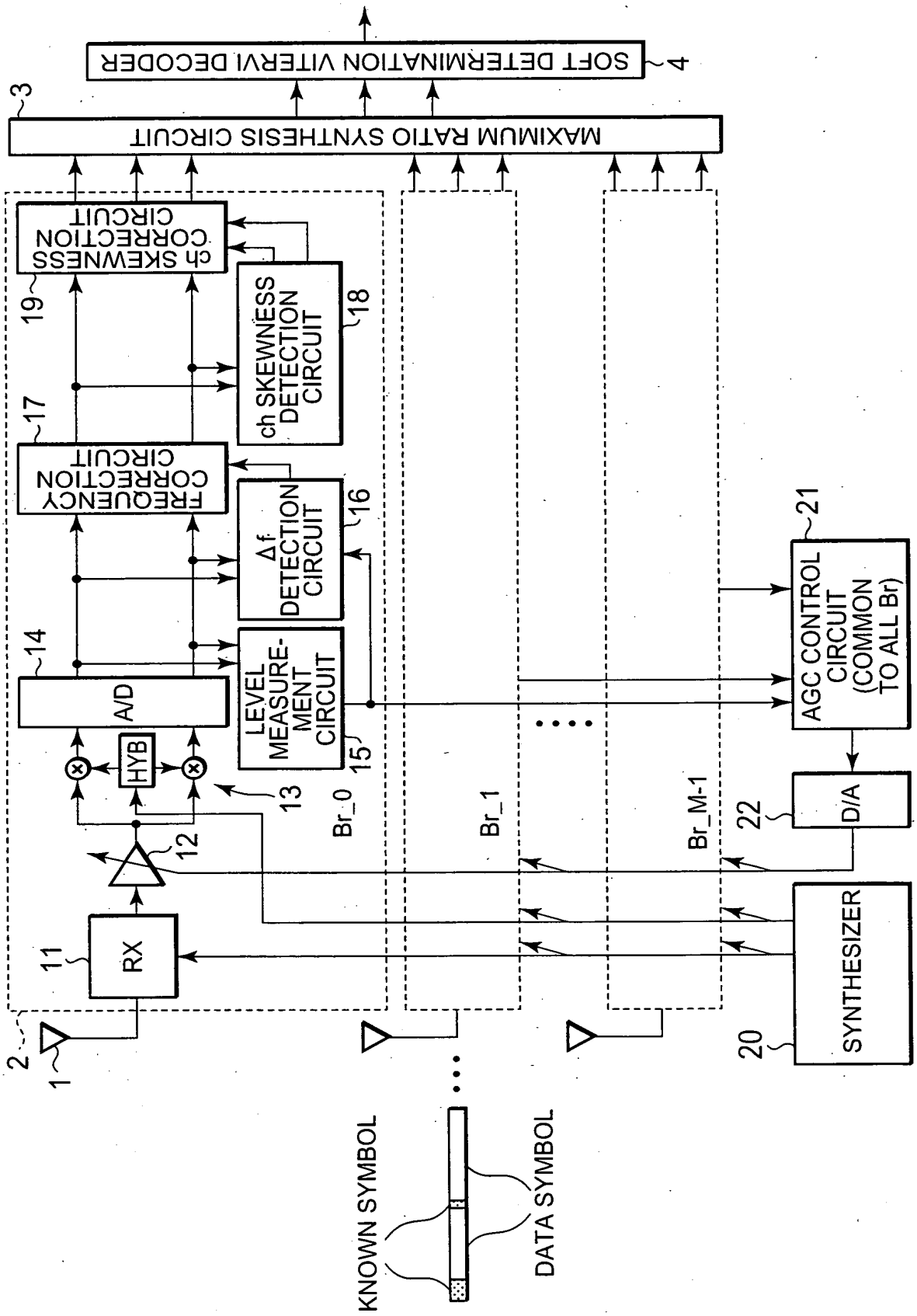

FIG. 8 PRIOR ART

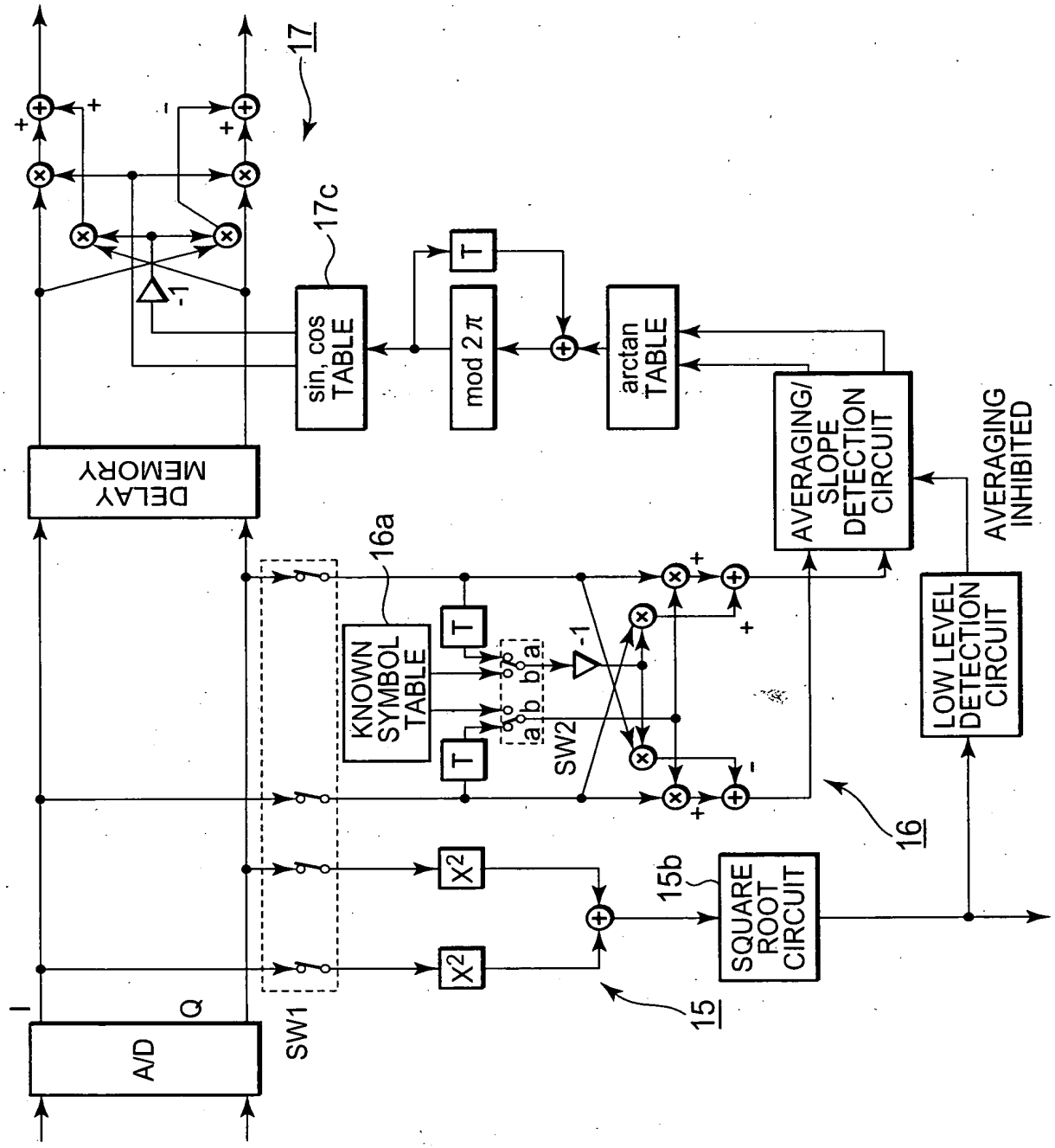

FIG. 9 PRIOR ART

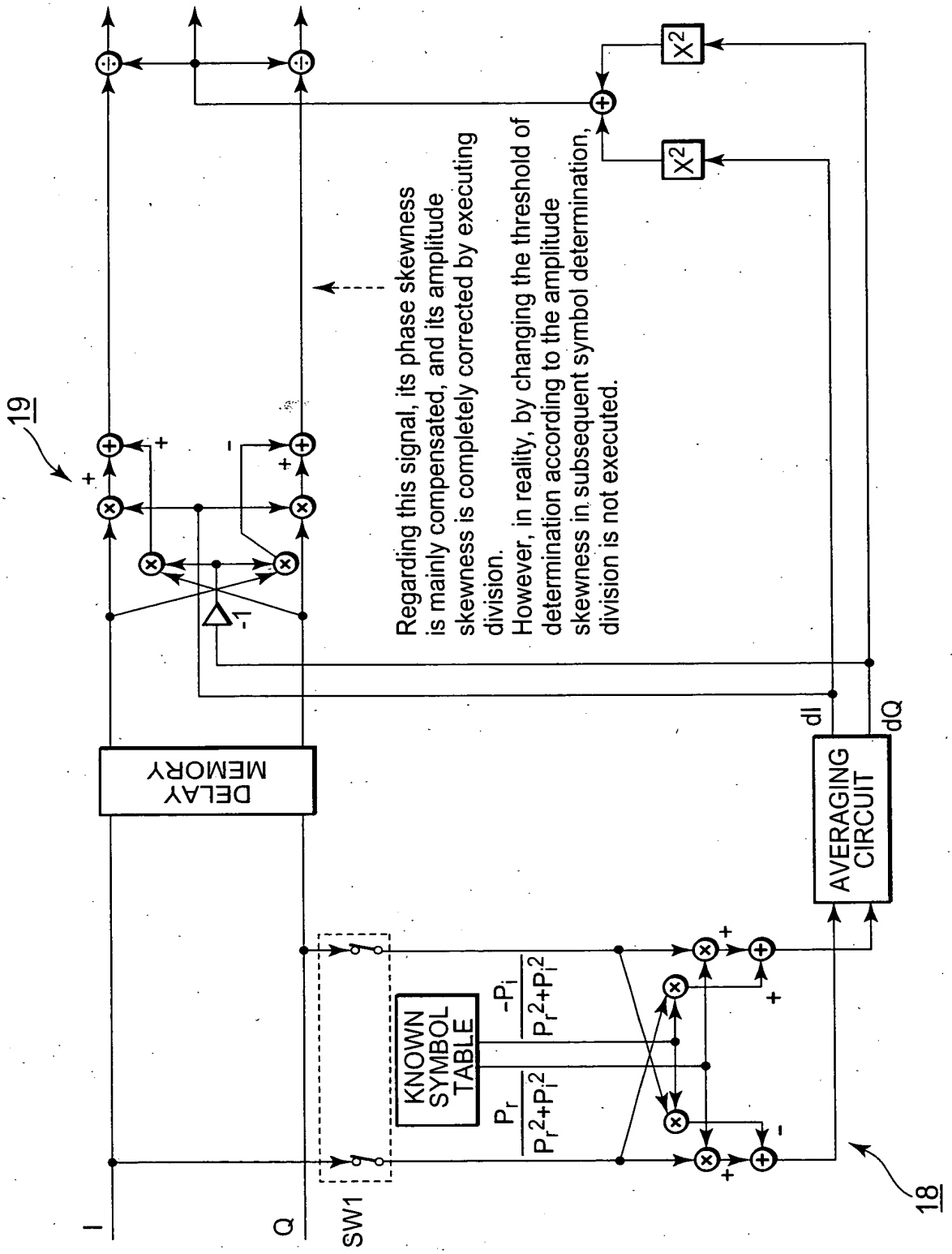
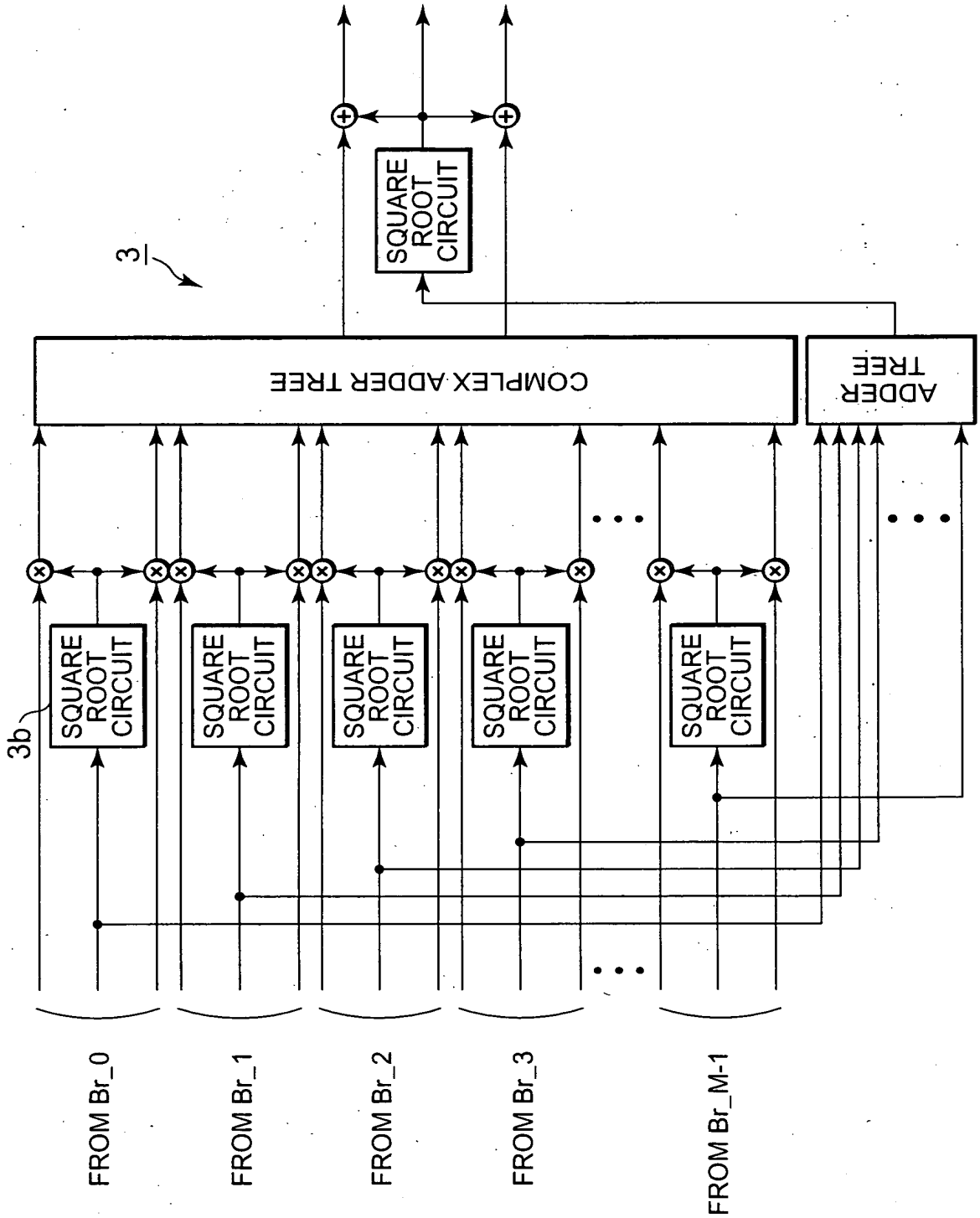
FIG. 10 PRIOR ART